IN THE SPECIFICATION:

(1) Please replace paragraph 12 on page 5 with the following paragraph showing changes.

In one embodiment of the present invention, the phase interpolator and the phase detector comprise a delay-locked loop (DLL). One possible architecture for a such a delay-locked loop is set forth in U.S. Patent Application Serial No. 09/947,488, filed on September 6, 2001 ~~[Attorney Docket No. LARSSON _ _]~~, entitled "Four Quadrant Analog Mixer-Based Delay-Locked Loop (DLL) for Clock and Data Recovery," that has now issued as U.S. Patent No. 6,586,977 and ~~which~~ is incorporated herein by reference.

(2) Please replace paragraph 25 on pages 10-11 with the following paragraph showing changes.

The in-phase and quadrature phase signals, I and Q, are provided to a phase interpolator 110. Though not necessary to the broad scope of the present invention, the phase interpolator 110 in the illustrated embodiment is an analog mixer-based phase interpolator. A first input signal S_{in-1} is provided to a clock generation circuit 135, and then to a phase detector (PD) 115. An output of the PD 115 is provided to the phase interpolator 110 along with the in-phase and quadrature phase signals, I and Q. The function of the clock generation circuit 135 will be discussed in detail with reference to FIGUREs 2 and 3. The phase interpolator 110, together with the phase detector 115, comprise a delay-locked loop (DLL), such as the DLL described in U.S. Patent No. 6,586,977 ~~co-pending patent application number [Attorney Docket No. LARSSON _ _], filed on [filing date], entitled "Four Quadrant Analog Mixer-Based Delay-Locked Loop for Clock and Data Recovery," and incorporated herein by reference~~. The benefits and advantages of clock and data recovery using

a DLL circuit of the type described therein are discussed in detail in the co-pending application, so that discussion will not be repeated here.